



MORPHEUS

Abstract of D3.1: Preliminary Architecture Definition

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ABSTRACT	This document is the abstract of the D3.1
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The MORPHEUS hardware architecture i.e. the MORPHEUS SoC is centred on three heterogeneous reconfigurable engines (HREs) targeting different types of computation:

- The PACT XPP is a coarse grain reconfigurable array primarily targeting algorithms with huge computational demands but mostly deterministic control- and dataflow. Further enhancements based on multiple, instruction set programmable, VLIW controlled cores featuring multiple asynchronously clustered ALUs also allow efficient inherently sequential bitstream-processing.
- The PiCoGA core is a medium-grained reconfigurable array consisting of 4-bit oriented ALUs. Up to four configurations may be kept concurrently in shadow registers. The architecture is mostly targeting instruction level parallelism, which can be automatically extracted from a C-subset language called Griffy-C.
- The M2000 is a lookup table based fine grain reconfigurable device – also known as embedded Field Programmable Gate Array (eFPGA). As any FPGA, it is capable to map arbitrary logic up to a certain complexity provided register and memory resources are matching the specifics of the implemented logic. The M2000 may be scaled over a wide range of parameters. The internals of a reconfigurable logic block may be modified to a certain degree according to the requirements. Flexibility demands may favour the implementation of multiple smaller M2000 eFPGAs instead of a single large IP. All control, synchronization and housekeeping is handled by an ARM 9 embedded RISC processor. As dynamic reconfiguration might impose a significant performance demand for the ARM processor, a dedicated reconfiguration control unit is foreseen to serve as a respective offload engine.

All system modules are interconnected via multilayer AMBA busses. Separate busses are foreseen for reconfiguration and/or control and data access. As the required bandwidth for high performance data intensive processing might become huge, it is planned to implement an additional circuit switched Network on Chip (NoC) which -with regard to the implementation- avoids the disadvantages of wide conventional bus systems. As NoCs imply a significant implementation risk, the AMBA busses will serve as proven fallback solution.

As the HREs operate on differing clock domains, they are decoupled from the system and interconnect clock domain by data exchange buffers (DEB) consisting of dual ported (dual clocked) memories either configured as FIFOs or pingpong buffers. The HREs have access to further onchip SRAMs for buffering of local data. These SRAMs may be either used as cache or scratchpad RAM. A state of the art multichannel SRAM/DRAM controller provides access to external system memories (volatile or non-volatile). All data transfers between HREs, on- and off-chip memories may be either HRE triggered or managed by a DMA control unit. Furthermore, a set of standard IO peripherals (UART, USB, timers, I2C etc.) is provided.

