



# MORPHEUS

## D6.10.1: Press release

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ABSTRACT This deliverable contains the text of the press release signalling the release of the MORPHEUS chip from foundry on February 6th. It also provides the corresponding dissemination means.  
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R1.1	19/01/2009	Creation	Done	Internal reviewers
R2.2	10/02/2009	Integration of reviewers comments	Done	Internal reviewers
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R3.1	11/02/2009	Integration of consortium remarks	Done	EB members
R3.5	17/02/2009	Modification	Done	WP1
R3.6	19/02/2009	Update of dissemination table	On going	General Assembly and EB members
R4.0	25/03/2009	Final update	Done	EC and reviewers

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## 1. Press release

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### **MORPHEUS leading edge reconfigurable SoC released from foundry**

Paris, February 6, 2009 – The MORPHEUS consortium led by THALES Research & Technology has announced the release of its reconfigurable chip from the STMicroelectronics foundry. It is the first silicon implementation of a single chip general-purpose architecture embedding fine-grained and coarse-grained dynamically reconfigurable hardware accelerators. The MORPHEUS chip, fabricated in 90 nm STMicroelectronics technology, is composed of complementary reconfigurable building blocks (PACT XPP-III, M2000 FLEXEOS, ST/ARCES PICOGA).

The various reconfigurable blocks mounted on the modular SoC design allow the platform to address the requirements of different applications. The reconfiguration of hardware blocks enables the optimization of a unified platform for different target applications: broadband wireless access, network routing, professional video and smart camera systems. The dynamic configuration provides designers, as well as end-users, with clear advantages in terms of flexibility, computing density and power consumption of the final application.

Reconfigurable blocks occupy around 64% of the overall area. The remaining area is shared between the processor, the communication infrastructure and bonding pads. The overall chip contains the equivalent of 8.5 million standard cell gates, 8.8 Mbits of embedded memory and a total of 97 million transistors. The chip is designed to operate chip level communication at a clock frequency of 200 MHz. Computation units operate on independent clock domains that can be dynamically switched to match each application real-time requirements, thus ensuring that power consumption is constantly maintained below the average estimated value. High computing performance is obtained through the massive parallelism of the reconfigurable blocks. Power consumption estimation is around 1W when all units operate at maximum frequency.

The next generation consumer and professional applications, terminals and networks will be built around flexible multipurpose hardware platforms. These platforms should allow high computing performance, low-power consumption and short time-to-market to quickly move from the designer's desk to the shop's shelves. Current solutions based on multiprocessing platforms do not meet these requirements, due to customizations specific to a single application domain or highly inefficient in terms of performance and power consumption. A major benefit of the MORPHEUS approach is that it introduces the ability to address new classes of embedded applications with extensive dynamic behavior. It is close to providing a general purpose platform via a clever mix of granularities and tools, providing flexibility beyond that offered by FPGA platforms.

MORPHEUS implements a "Soft-Hardware" platform to improve computing density, re-use, flexibility and time-to-market of the final applications. This is achieved through the design, prototyping and demonstration of a flexible platform based on reconfigurable architectures, along with the development of a dedicated tool chain for the management of the entire design flow. This integrated design flow accompanies the hardware platform, enabling designers to select the optimal application mapping after a rapid and accurate investigation among different implementation alternatives.

MORPHEUS stands for Multipurpose Dynamically Reconfigurable Platform for Intensive and Heterogeneous Processing. The overall budget is roughly 16 M€, of which 8.240 M€ are provided by the European Commission's FP6 program. The project was started in January 2006 and final results are expected in Q3 2009.

The MORPHEUS consortium includes 18 partners including large companies, universities and small and medium-sized enterprises from six European countries. The partners in the MORPHEUS project are: Thales Research & Technology, Deutsche Thomson OHG, INTRACOM Telecom Solutions, Alcatel-Lucent Deutschland AG, Thales Optronique SA, STMicroelectronics, PACT XPP Technologies, M2000 now Abound Logic, ACE Associated Compiler Experts, Critical Blue, University of Karlsruhe, Delft University of Technology, CEA-LIST, Université de Bretagne Occidentale, ARCES-University of Bologna, ARTTIC, Technical University Carolo-Wilhelmina zu Braunschweig and Technical University of Chemnitz.

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## 2. Appendix 1: Press release distribution

This press release targets actors (not necessarily experts) in the field of embedded systems computing solutions.

It will be disseminated through different means such as:

Dissemination means	Support	Date of diffusion	Audience targeted
<b>ICT Results</b> ( <a href="http://cordis.europa.eu/ictresults">http://cordis.europa.eu/ictresults</a> )	Identified by ICT results	March 2009	Embedded systems computing domain players
<b>PIDS</b> ( <a href="http://cordis.europa.eu/pids/">http://cordis.europa.eu/pids/</a> )	CORDIS	March 2009	European projects domain
<b>THALES TRT communication department</b>	THALES group web site	March 2009	THALES customers, etc
	"EDN" journal	March 2009	Electronics designers
	"Embedded Control Europe" journal	March 2009	Embedded systems people
	"Electronics Weekly" journal	March 2009	Electronics domain people
	"Semiconductor International" newsletter	March 2009	Semiconductor domain
	"Techonline" newsletter	March 2009	Advanced techniques interests
	"EE Times Newsletter"	March 2009	Electronics domain executives
<b>GDR CNRS ARS list</b>	E-mail list which contains about 500 e-mail addresses of scientists subscribers	16 March 2009	Academic community on architecture, compilation and parallelism
<b>BULLETINS-ELECTRONIQUES.COM (ADIT) – Veille technologique Internationale (technological watch)</b>	<a href="http://www.bulletins-electroniques.com/rechercher.htm">http://www.bulletins-electroniques.com/rechercher.htm</a>	23 March 2009	Scientific community
<b>CNRS International Journal</b>	Website and Revue <a href="http://www2.cnrs.fr/en/384.htm">http://www2.cnrs.fr/en/384.htm</a> <a href="http://www.cnrs.fr/inst2/">http://www.cnrs.fr/inst2/</a>	April 2009	Scientific community

### 3. Appendix 2: Thales Press release

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The Thales corporate communication department modified the text for publication through TRT communication department and for publication on the MORPHEUS web site.

#### MORPHEUS leading edge reconfigurable Chip released from foundry

**Neuilly sur Seine, March X, 2009** – The MORPHEUS consortium lead by Thales has announced the release of its reconfigurable chip from the STMicroelectronics foundry. It is the first silicon implementation of a single chip general-purpose architecture embedding fine-grained and coarse-grained dynamically reconfigurable hardware accelerators. The MORPHEUS chip, fabricated in 90 nm STMicroelectronics technology, is composed of complementary reconfigurable building blocks (PACT XPP-III, M2000 FLEXEOS, ST/ARCES PICOGA).

The dynamic configuration provides designers, as well as end-users, with clear advantages in terms of flexibility, computing density and power consumption of the final application.

High computing performance is obtained through the massive parallelism of the reconfigurable blocks. Power consumption estimation is around 1W when all units operate at maximum frequency. The overall chip contains the equivalent of 8.5 million standard cell gates, 8.8 Mbits of embedded memory and a total of 97 million transistors.

A major benefit of the MORPHEUS approach is that it introduces the ability to address new classes of embedded applications with extensive dynamic behavior. It is close to providing a general purpose platform via a clever mix of granularities and tools, providing flexibility beyond that offered by FPGA (*field-programmable gate array*) platforms.

#### **About MORPHEUS**

MORPHEUS stands for Multipurpose Dynamically Reconfigurable Platform for Intensive and Heterogeneous Processing. The overall budget is roughly 16 M€, of which 8.24 M€ are provided by the European Commission's FP6 program.

The MORPHEUS consortium is made of 18 partners including large companies, universities and small and medium-sized enterprises from six European countries. The partners in the MORPHEUS project are: Thales Research & Technology, Deutsche Thomson OHG, INTRACOM Telecom Solutions, Alcatel-Lucent Deutschland AG, Thales Optronique SA, STMicroelectronics, PACT XPP Technologies, M2000 now Abound Logic, ACE Associated Compiler Experts, Critical Blue, University of Karlsruhe, Delft University of Technology, CEA-LIST, Université de Bretagne Occidentale, Advanced Research Center on Electronic Systems of the University of Bologna, ARTTIC, Technical University Carolo-Wilhelmina zu Braunschweig and Technical University of Chemnitz.

#### **About Thales**

*Thales is a leading international electronics and systems group, addressing Aerospace and Space, Defence and Security markets worldwide. The Group's civil and military businesses develop in parallel and share a common base of technologies to serve a single objective: the security of people, property and nations. Thales's leading-edge technology is supported by 22,500 R&D engineers who offer a capability unmatched in Europe to develop and deploy field-proven mission-critical information systems. The Group builds its growth on its unique multidomestic strategy based on trusted partnerships with national customers and market players, while leveraging its global expertise to support local technology and industrial development. Thales employs 68,000 people in 50 countries with 2008 revenues of € 12.7 billion.*

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