

MORPHEUS



D4.3 Specification of the SoC implemented in WP4

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Context

This deliverable is part of the MORPHEUS project which is a European initiative financed under the 6th FP and addresses innovative solutions for embedded computing based on dynamically reconfigurable platform and tools.

MORPHEUS project aims at satisfying embedded systems new demanding requirements in terms of computing performance, cost-efficient development, functional flexibility and sustainability by developing a global solution based on a modular heterogeneous SOC platform providing dynamically reconfigurable computing completed by a software oriented design flow and a consistent toolset.

MORPHEUS is a 3 and a half -year project started in 2006 and gathering all the required expertises from several countries: academics, industrials, SMEs.

Aim of deliverable

This deliverable represents the final specification of the MORPHEUS chip. The chip will be used as demonstrator of the MORPHEUS architecture capabilities, and is one of the many possible configurations of the MORPHEUS computing platform.

Content of the deliverable

The document describes the final SoC configuration, and its organization. It provides all the physical details of the various components and it can be intended as the final chip datasheet as well as a specification document for the board integration.

For each of the main building blocks this document reports timing performance, area occupation, and power consumption of the database in relevant characterization corners: in particular

Power measurements for silicon proven macros have been provided.

- Timing evaluations are provided in Worst Case conditions, 0.9 V, 125C
- Power evaluations are provided in Nominal conditions, 1 V, 25C

Technology CMOS090 GP (High Speed, High leakage), 7metal layers, 2 threshold.

Area: The chip size is 110 mm², including Pads. HREs occupy around 64% of the overall area, the rest being divided between processor, communication infrastructure and 256 IO pads. The overall chip contains 8500 equivalent standard cell Kgates, 8831 Mbits of embedded memory cuts and a total number 97 Millions of transistor.

Timing: At the current status of the design, the target frequency for the processor based infrastructure for all design components is set to 100MHZ mark in worst case conditions (WCCOM 125C 0.9V) after place & route. Computational engines in the chip (Heterogeneous Reconfigurable Engines – HRE) are independent asynchronous clock islands. Their speed and consequently power consumption depends heavily on the mapped application. For this reason, each clock island features a software-programmable PLL to dynamically adapt HRE computation speed to the application specs and constraints. (M2K, XPP, DREAM, TOP)

Power Consumption: Power consumption estimation at this design stage (Gate-level netlist) is necessarily very inaccurate, especially for RTL logic, and floorplan-related IPs. Also, the selection of relevant application test-cases for power measurements is very difficult at half-way through the project. Preliminary evaluations show how leakage power for the chip should revolve around the 300 mW mark. Any evaluation on dynamic power consumption is necessarily related to floor-plan choices and in particular mode on the selection of a relevant application test-bench. This would have such a large impact on overall consumption, to the point that it would be more significant to evaluate separate power profiles for different application domains.