MORPHEUS

Abstract of D4.4:Report on structure of RTL code, resource budgeting

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ABSTRACT	This document is the abstract of the D4.4. It is available on the MORPHEUS public website
AUTHOR, COMPANY CONTRIBUTORS:	Fabio Campi, ST Eberhard Schueler, PACT, Gabriele Pulini, M2000 Tommaso DeMarco ST, Stefano Pucillo, ST, Antonello Deledda, ARCES, Florian Ries UK-ARCES Matthias Kuehnle, UK , Stephane Guyetant, CEA Sean Whitty, TUBS
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The present document describes a quantitative resource budgeting of the Morpheus architecture and its RTL database at the end of M18. The status of the design at this point is after final functionality specification, but prior to P&R feedback, memory sizes and HRE size fine-tuning, and final bug fixing after verification.

Timing: At the current status of the design, the target frequency for the processor based infrastructure for all design components is greater than the 250MHZ mark in worst case conditions (WCCOM 125C 0.9V) after logic synthesis. This is a viable prerequisite for closing the implementation phase at a target of 200MHZ, although the large area of the chip and the presence of IPs featuring large size may lead to floor-planning issues that may impact on final timing.

Computational engines in the chip (Heterogeneous Reconfigurable Engines – HRE) are independent asynchronous clock islands. Their speed and consequently power consumption depends heavily on the mapped application. For this reason, each clock island features a softwareprogrammable

PLL to dynamically adapt HRE computation speed to the application specs and constraints.

Area: The current area estimations suggest a chip size of ~90 mm_2, including Pads. HREs will occupy around 60 to 70% of the overall area, the rest being divided between processor, communication infrastructure and IO pads. This figure appears relevant in itself, but appears justified when compared to the overall computational power delivered by the Morpheus architecture. Further re-spins of the same architectural templates may offer space for optimization on timing [e.g. biasing threshold distribution according to feedbacks from measurements], whereas an optimization of the overall area above ~5/10% appears difficult without significantly impacting architectural choices or performance constraints.

Power Consumption: Power consumption estimation at this design stage (Gate-level netlist) is necessarily very inaccurate, especially for RTL logic, and floorplan-related IPs. Also, the selection of relevant application test-cases for power measurements is very difficult at half-way through the project. Preliminary evaluations show how leakage power for the chip should revolve around the 100 mW mark. This value may be significantly altered due to changes in threshold distribution in case the timing specs would prove very aggressive and timing closure for the architectural infrastructure or for the HREs would require massive use of low threshold logic. Any evaluation on dynamic power consumption is necessarily related to floor-plan choices and in particular mode on the selection of a relevant application test-bench. This would have such a large impact on overall consumption, to the point that it would be more significant to evaluate separate power profiles for different application domains. A significant contribution to overall dynamic consumption would also come from the chosen IO strategy: the inclusion of a high-speed large bandwidth memory controller will add a large overhead to the core power consumption that at the moment revolves around the 1.5 mW mark.

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